Amendments to the Specification:

Please amend paragraph number **[0007]** as follows:

[0007] Referring to FIGs. 1A through 1K, an exemplary, via-first, dual damascene process sequence is illustrated. It will be understood by those of ordinary skill in the art that the methods and structures described herein do not form a complete process for manufacturing ~~multi-level~~ multi-level ICs. The remainder of the process is known to those of ordinary skill in the art and, therefore, only the process steps and structures necessary to understand the conventional, via-first, dual damascene process sequence are described herein.

Please amend paragraph number **[0008]** as follows:

[0008] Referring to FIG. 1A, a cross-sectional view of a first intermediate structure 10 in the fabrication of a multi-level, dual damascene structure 34 (*see*, FIG. 1K) comprising an underlying copper metallization layer 12 (*e.g.*, a copper line or grounded copper contact) is illustrated. The first intermediate structure 10 includes a barrier layer 14 which resides on the underlying copper metallization layer 12. It will be understood by those of ordinary skill in the art that the figures presented in conjunction with this description are not meant to be actual ~~cross-sectional~~ cross-sectional views of any particular portion of an actual multi-level, dual damascene structure, but are merely idealized representations which are employed to more clearly and fully depict the conventional via-first, dual damascene process sequence than would otherwise be possible. Elements common between the figures maintain the same numeric designation.

Please amend paragraph number **[0012]** as follows:

[0012] Next, the via photoresist layer 22 may be removed (*e.g.*, using a plasma strip technique), as shown in FIG. 1D. The via 23 may subsequently be cleaned to remove any residual ~~photoreist~~ photoresist material and any dielectric etch material residues therefrom. In addition to preventing diffusion into, and enhancing adhesion to, the first interlevel dielectric layer 16, the barrier layer 14 also permits the via etch residues to be isolated from the underlying copper metallization layer 12, allowing the via 23 to be cleaned at this stage according to conventional techniques.

Please amend paragraph number **[0016]** as follows:

[0016] Once the barrier layer 14 has been punched-through beneath the ~~via 25,~~ via 23, the dual damascene structure 34 may be completed by forming a thin diffusion barrier 26 lining the bottom and sidewalls 23a and 25a~~, respectively,~~ of the via 23 and the trench 25, respectively, optionally forming a copper "seed" layer 28 over the diffusion barrier 26, depositing bulk copper 30 over the structure such that the trench 25 and via 23 are filled therewith (*see*, FIG. 1I) and planarizing the bulk copper 30 to stop on the surface of the second interlevel dielectric layer 20 using, *e.g.*, CMP (*see*, FIG. 1J). The dual damascene structure 34 may subsequently be completed by deposition of a thin cap layer 32 (*e.g.*, a silicon nitride cap layer) over the planarized bulk copper 30 and the second interlevel dielectric layer 20.

Please amend paragraph number **[0017]** as follows:

[0017] When the barrier layer 14 is etched (*see*, FIG. 1H), back-sputtering of copper onto the sidewalls 23a and 25a~~, respectively,~~ of the via 23 and the trench 25, respectively, or elsewhere on the structure, may occur. Additionally, post-etch residues from etching the dielectric layers 16 and 20 and the embedded etch stop layer 18 may remain as well. It is desirable to remove this contamination prior to completion of the metallization, *i.e.*, prior to deposition of the diffusion barrier 26. If not removed, the residues will remain trapped under the diffusion barrier 26. Residues, particularly copper residues, located on the wrong side of the diffusion barrier 26 may contribute to or cause device failure if, for instance, they diffuse into the dielectric layers 16 and 20.

Please amend paragraph number **[0021]** as follows:

[0021] The present invention, in one exemplary embodiment, includes a method for ~~post-etch~~ post-etch cleaning of multi-level damascene structures, which method minimizes, or substantially prevents, localized corrosion of underlying copper metallization. The method comprises subjecting an intermediate structure in the fabrication of a multi-level damascene structure, which structure includes an underlying copper metallization layer and an etched

opening (*e.g.*, a via) exposing at least a portion of the underlying copper metallization layer, to an aqueous or acidic wash solution, in an environment substantially shielded from ambient light, to substantially remove any post-etch residues which may be present on the sidewalls of the opening, or elsewhere on the structure. In one embodiment, the aqueous or acidic wash solution has a nonzero static etch rate when applied to both the copper and conventional dielectric materials, *e.g.*, silicon dioxide. An exemplary wash solution comprises about 7.0% by weight acetic acid, about 0.4% by weight nitric acid and about 0.15% by weight hydrofluoric acid. If this exemplary wash solution is utilized, the intermediate structure may be exposed to the solution for a period of time ranging from about thirty seconds to about two minutes, depending upon the amount of residue to be removed therefrom.

Please amend paragraph number **[0025]** as follows:

[0025] The present invention is directed to a method for the post-etch cleaning of ~~multi-level,~~ multi-level damascene structures having underlying copper metallization. The method provides a way in which localized, photo-induced corrosion of copper metallization underlying etched openings in damascene structures may be minimized, or substantially prevented, while permitting the use of aqueous or acidic wash solutions to clean the structures. The particular embodiments described herein are intended in all respects to be illustrative rather than restrictive. Other and further embodiments will become apparent to those of ordinary skill in the art to which the invention pertains without departing from its scope.

Please amend paragraph number **[0026]** as follows:

[0026] The method of the present invention comprises subjecting an intermediate structure in the formation of a ~~multi-level,~~ multi-level damascene structure, which intermediate structure includes an etched opening therein through which at least a portion of an underlying copper metallization layer is exposed, to an aqueous or acidic wash solution, in an environment substantially shielded from ambient light, to remove any residues which may be present on the sidewalls of the etched opening, or elsewhere on the intermediate structure. One example of such an intermediate structure is the intermediate structure 36 shown in FIG. 1H.

Please amend paragraph number **[0030]** as follows:

[0030] In practice, the structure to be cleaned, which structure typically would include a plurality of vias and trenches etched therein, would be placed in a reduced ambient light chamber which preferably completely shields and isolates the structure from all ambient light and the aqueous/acidic wash solution would be applied to the etched surfaces thereof for a period of time (in the case of the acetic/nitric/hydrofluoric acid wash solution discussed above) ranging from about thirty seconds to about two minutes. Again, the duration of exposure to the wash solution would depend upon the amount of residue to be removed from the structure. The structure would subsequently be removed from the chamber and a diffusion barrier ~~layer~~ 26 formed thereover, as previously discussed, followed by an optional seed layer 28 and a bulk copper layer 30. It is currently preferred that the structure remain in reduced ambient light conditions until the diffusion barrier ~~layer~~ 26 is formed over the exposed portion of the underlying copper metallization layer 12 to further minimize photo-induced corrosion thereof.